

# Simulating Battery Packs Comprising Parallel Cell Modules and Series Cell Modules

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## Abstract

EV and HEV battery packs require cells connected both in parallel and in series. It is impractical to build a monolithic pack where all cells are connected together in a matrix; instead, packs are built using smaller modules. The “parallel cell module” approach wires cells within a module in parallel, and then wires modules in series; the “series cell module” approach wires cells within a module in series, and then wires modules in parallel. This paper addresses economic and technical advantages and disadvantages of both. We describe a simulation system developed to evaluate different scenarios, and present some preliminary findings.

*Keywords: simulation, battery, battery model, EV (electric vehicle), HEV (hybrid electric vehicle)*

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## 1 Introduction

Battery packs for EV or HEV applications (or anything in the continuum in-between, which we collectively call “xEV”) require many individual cells connected both in parallel (to generate high current source/sink capability) and in series (to develop high voltage). It is generally impractical to build a monolithic pack where all cells are connected together in a matrix form. Instead, packs are composed of smaller modules of cells. There is great variety in how these modules may be configured, but the two extreme cases are (1) cells within any specific module are wired in parallel (and the modules themselves wired in series), or (2) cells within any specific module are wired in series (and the modules themselves wired in parallel, connected at their output terminals only). We call these two cases the “parallel cell module” (PCM) and the “series cell module” (SCM) approaches, respectively.

This paper first discusses economic tradeoffs between the two approaches, and then presents some preliminary findings on the performance of PCM versus SCM, based on a simulation system developed in MATLAB [1] for that purpose. The goal is to understand the advantages and disadvantages of the two approaches to better inform

design decisions. The simulator itself is also described.

## 2 Comparing PCM and SCM

A battery pack designer faces a number of constraints, both external (e.g., performance requirements, packaging volume, durability, cost) and internal to the pack (e.g., cell limitations, available space). As we will find after discussing these constraints, there are a number of options available to the pack designer within a given pack architecture, with one key option being the PCM. Its benefits include ease of design re-use, pack expandability, and simpler control and monitoring. A potential disadvantage includes lower fault tolerance (single-point failure). A second key option is SCM. Its advantages include: the ability to add capacity without changing the system voltage, tolerance to a single-point “open” failure, and a more precise match between available cells and overall pack capacity. Its disadvantages include: the need for more complex balancing circuitry, and extra care required when servicing high-voltage modules versus low-voltage modules. In the following two sections, we consider (1) external and internal pack design constraints, including: required voltage, capacity,

and power; and (2) pack architecture considerations.

## 2.1 Pack Design Constraints

Three fundamental performance requirements for all xEV battery packs are: operating voltage (e.g., nominal voltage or  $V_{nom}$ , with operating boundaries of  $V_{min}$  and  $V_{max}$ ), capacity (in ampere-hours, or Ah), and power (in watts, or W). These are discussed in the following subsections.

**Voltage constraints:** The required operating voltage at the pack level (that is, at the output terminals of the complete battery pack) is typically specified by the integrator of the electric drive components, and is a function of the voltage and current-carrying capabilities of the drivetrain components. Within the battery pack, the lowest discrete voltage is that of the individual cell, as determined by its electrochemistry. For the purposes of this paper, we assume lithium-ion polymer cells, with  $V_{nom} = 3.75V$ ;  $V_{min} = 2.5V$ ,  $V_{max} = 4.2V$ . Therefore, the battery pack for a typical high voltage xEV application ( $V_{nom} = 360V$ ) requires the equivalent of 96 cells connected in series.

**Capacity constraints:** The performance of pure Electric Vehicles (EVs), Plug-in Hybrid Electric Vehicles (PHEVs), and HEV systems with Electric Auxiliary Power Units (EAPUs) is strongly dependent on the capacity rating of the battery packs. The higher the capacity, the farther the vehicle can travel solely on electric power without recharge, or the longer the EAPU can operate without recharge. Within the battery pack, the lowest discrete element of capacity is, again, that of the individual cell. Unlike cell voltage (which is fixed by virtue of the reduction potentials of the half reactions of the particular electrochemistry), cell capacity is determined largely by the physical construction of the cell, and therefore cells of different (but fixed) capacities are possible. A typical high-capacity cell is actually a collection of multiple anode/cathode pairs connected in parallel within the cell.

Increasing the capacity of a cell can be accomplished in a number of ways:

- Increasing the number of anode/cathode pairs in a cell;
- Increasing the thickness of the active material on the cathodes;
- Increasing the size (area) of the electrodes; or,
- Combinations of the above.

However, there are certain practical limitations on cell capacity growth (details of which are beyond the scope of this paper), and the high incremental cost of manufacturing multiple, unique capacity cells means the battery pack designer generally is limited to one or two capacities to choose from. Moreover, cells of different capacities cannot be mixed within a pack, and therefore the designer must choose one cell for a given battery pack. If the capacity requirements of the application exceed the capacity of the chosen cell, then two or more cells must be “combined” in parallel (see section 2.2). For example,

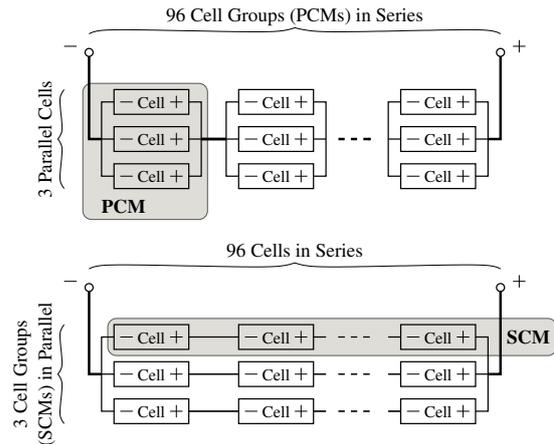


Figure 1: An example 288-cell pack comprised of 96 PCMs (top) or 3 SCMs (bottom).

if a PHEV application requires 30Ah capacity, and 10Ah cells are available, then 3 parallel cells would be required. If 15Ah cells are available, then only 2 parallel cells would be required.

As an aside, this presents an additional constraint on the cell manufacturer: creating a cell of very high capacity will result in wasted capacity, volume, and mass if the required pack capacity is not an integer multiple of the cell’s capacity.

**Power constraints:** Performance requirements for standard HEVs generally focus on the power capabilities of the battery pack, rather than capacity, and therefore battery packs for HEVs typically do not require paralleling of cells. Performance requirements for EVs and PHEVs, on the other hand, are dominated by capacity needs.

## 2.2 Pack Architecture Considerations

For the purposes of this paper, “pack architecture” refers to the particular electrical (schematic) interconnection of the individual cells. In this section, we will use the example of a 360V, 30Ah PHEV system for which a 10Ah, 3.75V battery cell is available for use by the pack designer. To meet the specified performance requirements, the battery pack would require three cells in parallel and 96 cells in series, for a total of 288 cells.

Two possible approaches for designing this battery pack are shown in Fig. 1. The PCM approach (top of figure) builds modules by wiring three cells in parallel (with a combined capacity of 30Ah), and then builds the pack by wiring 96 modules in series (for a nominal pack voltage of 360V). The SCM approach (bottom of figure) builds modules by wiring 96 cells in series, and then builds the pack by wiring three modules in parallel.

The PCM approach has a number of advantages:

1. If cells are reasonably balanced when connected in parallel, connecting the trio of cells directly in parallel enhances their ability to stay balanced throughout the life of the pack. That is, within a nominal range they “self-balance”. This is somewhat intuitive since, after all, a typical battery cell is itself a collection on parallel-connected electrodes.

2. If a PCM for some reason falls out of balance compared to other PCMs, forced balancing is straightforward since each PCM can be balanced independently of the others.
3. Assembling and servicing battery packs which are configured with a PCM architecture is somewhat safer than alternative architectures, because the nominal voltage of the assemblies to be connected in parallel is nominally 3.75V. If the cells are even 20% out of balance, the voltage difference at the instant of connection would be less than 0.8V.
4. No complex switching or voltage normalization circuitry is needed to add more modules to a pack.
5. The ability to connect cells as PCMs potentially allows a more precise match between available cells and overall pack capacity

One disadvantage to the PCM approach is the single-point failure condition where all cells in one PCM fail “open,” breaking the series chain. However, this failure mechanism exists for any series-connected string of cells (except SCM, as described below). In fact, for the case of one of the three cells failing “open” in a series-connected PCM pack, the other two cells would maintain continuity, and, assuming appropriate monitoring and control, the battery pack’s management system could allow the pack to continue to operate, albeit it at a lower performance, until the failed PCM is replaced. Another potential failure mode is where one cell in the trio fails as a short circuit. This could cause overheating as the other parallel cells then dump energy into the shorted cell. The ability of the cells to withstand such overstress becomes a critical cell design element. We have seen that PCMs of up to three cells can withstand this failure without serious damage. Extending the size of the PCM to more than three requires additional experimentation.

The SCM architecture has some advantages over PCM architecture, particularly if extremely high capacities are required (e.g., >50Ah); most notably, the ability to add capacity without changing the system voltage. Consider, for example, the case of vehicle manufacturer who wishes to offer a range of battery capacities: the base vehicle could be offered with one pack consisting of 96 series-connected cells (360V, 10Ah capacity). To double the vehicle’s driving range, the ability to attach a second pack in parallel with the first would satisfy this desire with minimal additional investment, since there would be no need to alter the vehicle’s electric drive circuitry. Another advantage of the SCM architecture is the tolerance to a single point “open” failure. Assuming two or more SCMs are installed, if one SCM opens, the other SCM can continue to operate the vehicle, although at lower capacity. A shorted cell would merely reduce the SCM voltages by one cell voltage, or approximately 1%. Finally, as with the PCM architecture, being able to connect SCMs in parallel allows for a more precise match of between available cell capacities and overall desired pack capacity.

Some disadvantages to the SCM architecture, however, include:

1. More complex intra-SCM cell balancing circuitry may be needed, due to the higher overall voltages generated in an SCM.
2. Assembling and servicing packs requires special switching and voltage balancing circuitry to ensure that the difference between SCM voltages is within safe tolerances prior to connecting in parallel. A 20% voltage deviation in a 360V SCM is 72V, for example.

## 3 PCM and SCM Simulators

### 3.1 The PCM simulator

To be able to make a fully informed decision re. PCM versus SCM, it is important to be able to test their responses to typical usage and fault conditions. We have developed simulator systems in MATLAB to do so for the PCM and SCM approaches. To the best of our knowledge, the only other literature on simulating battery packs using a cell model is in [2,3], where battery-pack modeling is more in view than is battery pack performance for different cell and module configurations.

Our simulator system models all cells within the pack using the “enhanced self-correcting” (ESC) cell model. This model is well described in [4–6], so we simply state here that it includes contributions due to polarization voltages, hysteresis voltages, ohmic voltages, and open-circuit voltages with sufficient accuracy to be valuable for this purpose. The model has a structure that is important for the simulation method to be practical, which is:

$$\begin{aligned} x_k &= f(x_{k-1}, i_{k-1}, T_{k-1}) \\ y_k &= \underbrace{\text{OCV}(z_k, T_k) + Cf_k + Mh_k}_{\text{Not directly dependent on current}} + i_k R. \end{aligned}$$

The first equation is the state equation, which updates the dynamics of the model state vector  $x_k$ . The present state is a function of the prior state  $x_{k-1}$ , the input current value  $i_{k-1}$  and the cell temperature value  $T_{k-1}$ . The state vector includes state-of-charge (SOC)  $z_k$ , the polarization voltages  $f_k$ , and hysteresis  $h_k$ . The second equation is the output equation and calculates a cell terminal voltage  $y_k$  based on open-circuit-voltage (OCV), polarization voltages, hysteresis, and ohmic voltage.

Given known input current and temperature for a specific time step, the model equations describe how to update the model state and output voltage for that time step. Therefore, to be able to update the models for all cells in a pack, the individual cell input currents and temperatures are needed. Cell temperatures and *pack* currents are the inputs to the simulator. Cell current is found from pack current by realizing that current through every PCM is identical; therefore, the only challenge is to determine how the current is split among the individual cells in each PCM.

A fact that is critical to understand for an efficient implementation of this simulator is that neither the present value of the polarization voltage nor the present value of hysteresis depend on the

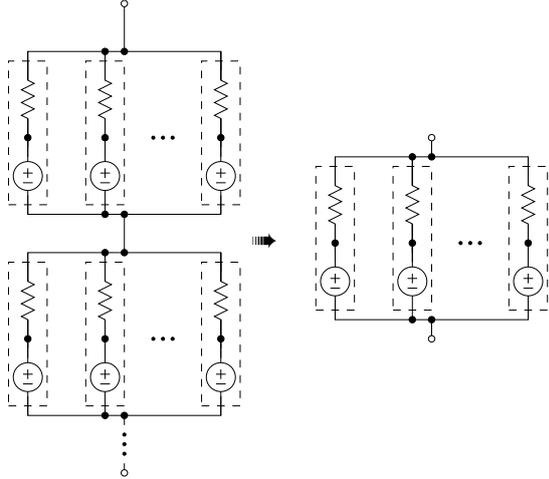


Figure 2: A battery pack (on the left) comprising parallel-cell-modules (right).

present value of input current. Therefore, cell terminal voltage, computed via the output equation, simply comprises a lumped constant voltage  $v_k = \text{OCV}(z_k, T_k) + Cf_k + Mh_k$  plus an ohmic term  $i_k R$ . The simulator uses this cell model to simulate packs with  $N_s$  modules wired in series, where the modules comprise  $N_p$  cells wired in parallel. Each PCM has  $N_p$  voltage sources and  $N_p$  resistances. A PCM-based pack is drawn in the left frame of Fig. 2. The relevant consideration here is a single PCM (shown in the right frame of Fig. 2) where each cell has a voltage source and a resistance.

We label the resistance of cell  $j$  at time  $k$  as  $R_{j,k}$ . Similarly, each cell voltage source is labeled  $v_{j,k}$ . The PCM voltage is  $v_k$ , the cell currents are  $i_{j,k}$ , and the externally applied current is  $i_k$ . From circuit analysis, we know that the sum of currents entering each cell must equal the externally applied current. This gives:

$$i_k = \frac{v_k - v_{1,k}}{R_{1,k}} + \frac{v_k - v_{2,k}}{R_{2,k}} + \dots + \frac{v_k - v_{N_p,k}}{R_{N_p,k}}$$

$$v_k = \frac{i_k + \sum_{j=1}^{N_p} \frac{v_{j,k}}{R_{j,k}}}{\sum_{j=1}^{N_p} \frac{1}{R_{j,k}}}.$$

We use pack current to determine PCM voltage. Once we know the PCM voltage  $v_k$ , it is simple to determine the branch currents as  $i_{j,k} = (v_k - v_{j,k})/R_{j,k}$ . Given the branch currents, we can update each cell model in the pack simulation.

In the simulator, the cells may have individual capacities, resistances, and starting SOC levels. Unless otherwise stated, however, the following characteristics are assumed: A room-temperature OCV characteristic based on a high-energy LiPB cell comprising a spinel cathode and a blended-carbon anode, a cell resistance of 2.5 m $\Omega$ , and a cell capacity of 9Ah.

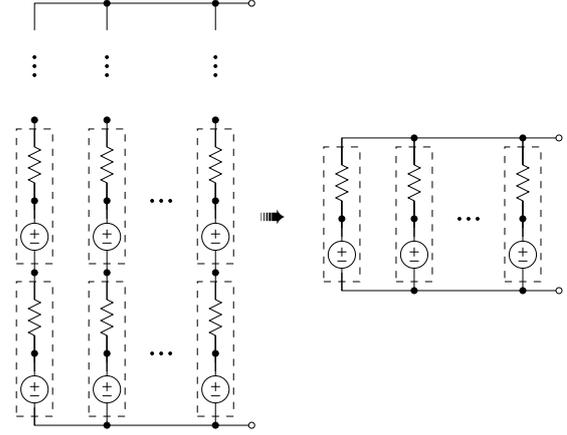


Figure 3: A battery pack (on the left) comprising series-string-cell-modules. On the right, an equivalent-circuit representation of the battery pack.

### 3.2 The SCM simulator

We have also developed a simulator system in MATLAB to be able to evaluate the SCM approach from a technical viewpoint. Again, the simulator models all cells within the pack using the ESC cell model. As before, to be able to update the models for all cells in a pack, the individual cell input currents and temperatures are needed. Cell temperatures and pack currents are the inputs to the simulator. Cell current is found from pack current by realizing that current through every cell in any given SCM is identical; therefore, the only challenge is to determine how the pack current is split among the SCMs.

Cell terminal voltage comprises a lumped constant voltage  $v_k = \text{OCV}(z_k, T_k) + Cf_k + Mh_k$  plus an ohmic term  $i_k R$ . The simulator uses this cell model to simulate packs with  $N_s$  cells wired in series, comprising modules, and  $N_p$  modules wired in parallel. Each SCM then has  $N_s$  lumped voltage sources and  $N_s$  resistances as drawn in the left frame of Fig. 3. Standard circuit analysis techniques can reduce this to an equivalent circuit (shown on the right) where each SCM has a voltage source (equal to the sum of the original lumped voltages in that SCM) and a resistance (equal to the sum of the resistances in that SCM). We label the total resistance of the  $j$ th SCM at time  $k$  as  $R_{j,k}$ . Similarly, we label the total lumped voltage source of the  $j$ th SCM at time  $k$  as  $v_{j,k}$ . The overall bus voltage is  $v_k$ , the SCM currents are  $i_{j,k}$ , and the externally applied current is  $i_k$ . From circuit analysis, we know that the sum of currents entering each SCM must equal the externally applied current. As before, this gives:

$$v_k = \frac{i_k + \sum_{j=1}^{N_p} \frac{v_{j,k}}{R_{j,k}}}{\sum_{j=1}^{N_p} \frac{1}{R_{j,k}}}.$$

Therefore, we use demanded pack current  $i_k$  to determine bus voltage  $v_k$ . Once we know the bus voltage, it is simple to determine the SCM currents as  $i_{j,k} = (v_k - v_{j,k})/R_{j,k}$ . Given the SCM

currents, we can update each cell's model in the pack simulation.

### 3.3 Basis of operation of the simulators

The PCM and SCM simulators are quite straightforward. They maintain (separately for all cells in the pack, and for every simulation iteration) values for SOC, hysteresis level, polarization voltage states, resistance and capacity. These may be initialized in various ways in order to define different simulation scenarios. Unless otherwise mentioned, SOC values are initialized to 50%; hysteresis levels to zero; polarization voltage states to zero; resistances to 2.5 m $\Omega$ , and cell capacities to 9Ah. A room-temperature OCV characteristic based on a high-energy LiPB cell comprising a spinel cathode and a blended-carbon anode is used for all simulations.

**In the PCM simulator:** Every iteration of the simulation, the following actions are performed. The lumped voltage of each cell is computed, including contributions due to OCV, polarization voltages, and hysteresis voltages, which are later updated using the ESC cell model. Given the pack current as an input, the individual PCM voltages are then computed, and from that the individual cell currents within each PCM are computed. If PCM equalization is "on," cell currents are modified as necessary (i.e., if the PCM-average SOC is above the minimum PCM SOC by at least 0.5%, an additional discharge current is added to that PCM).

**In the SCM simulator:** Every iteration of the simulation, the following actions are performed. The lumped voltage of each cell is computed, including contributions due to OCV, polarization voltages, and hysteresis voltages, which are later updated using the ESC cell model. SCM lumped voltages are computed as the sum of all lumped voltages in any given SCM; SCM lumped resistances are computed as the sum of all resistances in any given SCM. Given the pack current as an input, the bus voltage is computed, and from that the individual SCM currents are computed. Cell currents are assigned to the SCM current for the SCM containing that cell. If intra-SCM equalization is "on," cell currents are modified as necessary (i.e., if the cell SOC is above the minimum cell SOC in that SCM by at least 0.5%, an additional discharge current is added to that cell).

**In both simulators:** Once adjusted cell currents are available, the ESC cell model for each cell is updated. That is, the SOC state, the hysteresis state, and the polarization voltage states are updated. These are stored for the next iteration of the simulation loop.

The pack tests described herein have a pack current of either 0A (pack is resting), or they cycle the pack from a low SOC value to a high SOC value and back again (repeatedly). For the cycling tests, the cell SOC's are all checked at the end of every simulation step: if any SOC is below the lower limit of 5%, the sign of the pack current is changed from discharge to charge; if any SOC is above the upper limit of 95%, the sign of the pack current is changed from charge to discharge.

## 4 Simulation Results for PCM

This section discusses preliminary findings obtained by using the PCM simulator. Our biggest concern technically was whether we would see large SOC differences between different PCMs or large cell currents in PCMs with cells having different capacities, resistances, leakage currents, and so forth. (Large SOC differences within a pack can lead to under-utilization of the pack's full charge/discharge range, and large current differences can lead to unequal and premature aging of cells.) The following subsections present tests under various permutations of rate profile, initial SOC, cell resistance, cell capacity, and cell faults. The majority of the results in this section are for PCMs comprising four cells wired in parallel, and packs comprising four PCM units wired in series. While this pack is smaller than one that would be used in practice, it demonstrates the behaviors that we would see in a larger pack in ways that are easier to plot and therefore to visualize. The results are then also more comparable to the SCM plots shown later for a pack having the same total number of cells in the dual arrangement.

### 4.1 The pack at rest

The first simulations considered what would happen if the cells in the pack were initialized to different SOC values, and the pack was allowed to rest. This is not a very realistic scenario as cells within a PCM tend to self-equalize (as we will soon see), so we would not expect to encounter largely divergent SOC values within any particular PCM. However, it is a good test to see whether the simulator is giving reasonable results. It is also indicative of how cells within a PCM will self-equalize should their SOC's differ when they are initially connected.

If cells are initialized to disparate SOC's, their OCV's will likewise be different. Cells in a PCM having relatively higher OCV will discharge into cells having relatively lower OCV until the voltages of all cells within any PCM are identical. (Since cell voltage is assumed to comprise OCV plus polarization voltages plus hysteresis, and polarization voltages decay to zero upon a cell resting, the lumped cell voltages in each cell, comprising OCV plus hysteresis, must be equal. As hysteresis is a fairly small effect at room temperature, SOC's will be nearly equal but not necessarily identical in a PCM at equilibrium.) The terminal voltages of each cell behaves something like an RC (resistor-capacitor) circuit. Small resistances allow larger currents (for the same voltage difference) and hence faster adjustment; larger resistances cause slower adjustment. Fig. 4 shows results for this experiment, where cells are assigned random initial SOC values between 40% and 60%. [All plots in this paper are best viewed in color.]

The left plot shows the progression of cell SOC versus time for all cells in the pack, organized according to the PCM in which the cells are located. The middle plot shows the current versus time for each cell. (In this case, the pack load current is zero, but there is current that circulates between the cells in each PCM as high-voltage

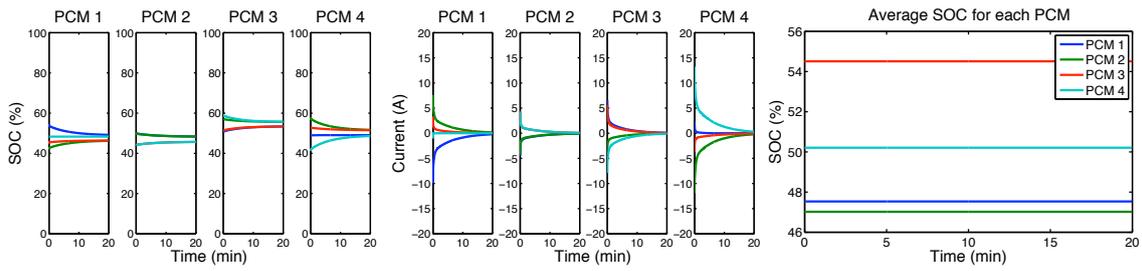


Figure 4: Resting pack (random initial SOC values).

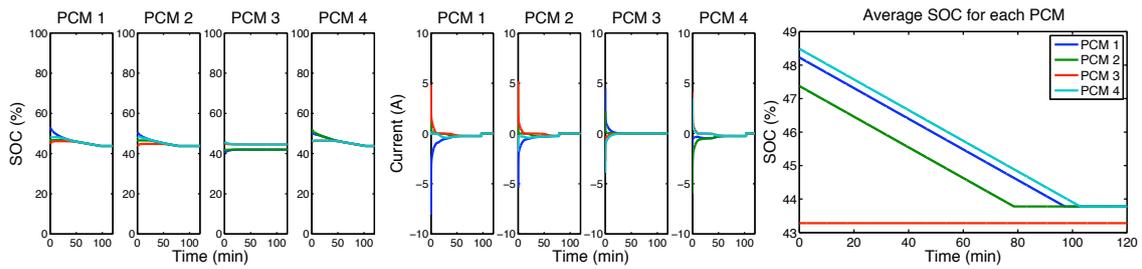


Figure 5: Resting pack with PCM equalization "on" (random initial SOC values).

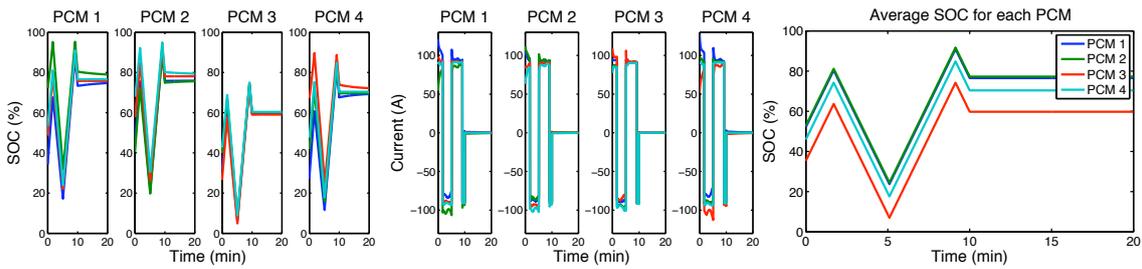


Figure 6: Cycling pack at 10C rate (random initial SOC values).

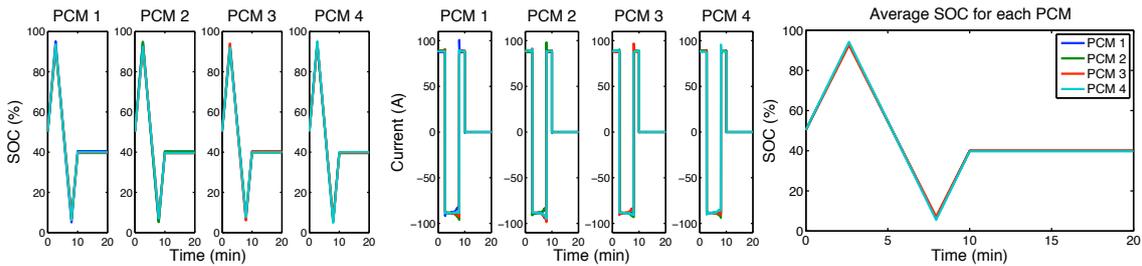


Figure 7: Cycling pack at 10C rate (random initial capacity values).

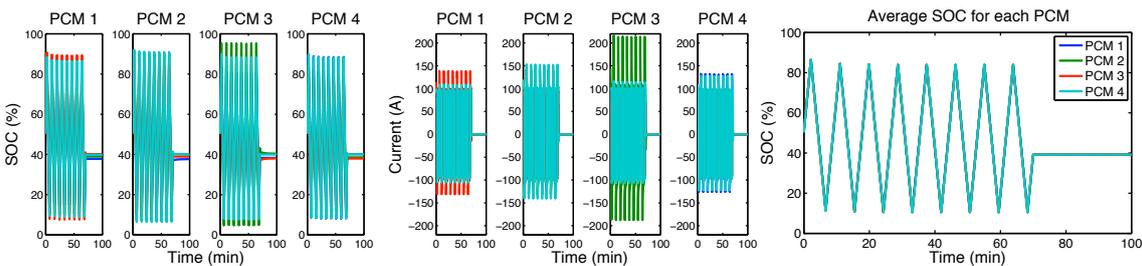


Figure 8: Cycling pack at 10C rate (random resistance values).

cells discharge into low-voltage cells.) The right plot shows the PCM-average SOC versus time for the four PCMs. These plots come from a single simulation run with a single set of random initial cell SOC, but are representative of the effects that we observe over repeated runs. [All simulations in this paper have the same reporting format as is presented in Fig. 4.] In this test, cell equalization is “off” (no individual cell “boost” or “buck” circuitry). Therefore, PCMs maintain their relative separation in SOC from each other. This effect is evident in the right plot. And as previously mentioned, although voltages equalize within a PCM, SOC do not converge to identical values due to hysteresis in the cell dynamics. In the next test, cell equalization was turned “on”. The results of that test are shown in Fig. 5. Cells were initialized with SOC ranging from 40% to 60%. As the simulation ran, PCMs having SOC higher than the lowest PCM SOC were “bucked”. That is, a constant-current load was placed across the terminals of those PCMs. The bucking current was set to 1A in these tests, which is higher than we would implement in practice. However, it shows the same effects that we would expect to see for lower bucking currents, at a faster time scale. Since all PCMs in the pack are considered when selecting the PCMs to buck, we see that the disparity in SOC values between different PCMs is eliminated by bucking. (In order to minimize stress to the cells, bucking current for any PCM was turned off when that PCM’s SOC was within 0.5% of the lowest SOC in the pack. Hence, the final divergence in SOC between highest SOC and lowest SOC is 0.5%. This is a user-specified parameter, and can be changed to any desired value.)

#### 4.2 Varying initial SOC

The second test that we consider maintains a constant resistance and a constant capacity per cell, again initializes each cell with a random SOC, but then cycles the pack with constant-current charge and discharge pulses. The magnitude of the pulses used in the simulation is 10C (about 360A). While a 10C pulse is quite large, especially if an EV pack is being considered, it speeds the simulation. In certain cases the higher current can lead to magnified effects, as we will see later, but that is not the case here. (Charging was stopped when the maximum cell SOC reached 95%, and discharging stopped when the minimum cell SOC reached 5%). After 10 min, the pack was allowed to rest. Equalization was again “turned off.” Results typical of this scenario are presented in Fig. 6.

The most important aspects of these results are essentially identical to those of the “rest” case just presented. Namely, within each PCM, cell SOC converge to values close to each other, even in a dynamic setting. (When equalization is turned on, the results were essentially the same, except that the PCM-average SOC deviation slowly decreases.) Cell currents within a PCM differ primarily because of the nonlinear OCV relationship: cells at different SOC points but having otherwise identical state have different terminal voltages.

#### 4.3 Varying Capacity

The third test that we consider maintains a constant resistance and initial SOC (of 50%) for each cell, but gives each cell a random capacity uniformly chosen between 8.5Ah and 9.5Ah. The pack is then cycled.

Results from this test are shown in Fig. 7. While all cell SOC start with the same value, they diverge in value as the PCM SOC approach their upper and lower limits due to differing cell capacities. In this case, the magnitude of the divergence is around 2%.

Decreasing the pulse constant-current level from 10C to 1C had an interesting effect. Within PCMs, the SOC still tend to diverge as the pack is cycled, but there is a self-correction that happens as well. The applied pack current tends to de-equalize cells having different capacities since their SOC change at different rates. However, the parallel connections within each PCM maintains equal terminal voltage of all cells and tends to equalize SOC. PCM self-equalization was easier to accomplish with the lower pack current because relatively more “equalizing” could be done—the rate of inter-PCM equalization is unchanged, but the rate of de-equalization was reduced. We note that the overall level of intra PCM SOC disparity is less than before.

#### 4.4 Varying resistance

The fourth test that we consider maintains a constant capacity and initial SOC (of 50%) for each cell, but varies the resistance. The simulator permits very complex models of resistance as a function of SOC, but we begin here with the assumption that resistance is constant but different for each cell, distributed uniformly between 1mΩ and 4mΩ. We again begin with a high-rate simulation, with results presented in Fig. 8.

One cell in PCM 3 randomly received a resistance value that was much lower than that of the other cells in that PCM. The consequence of this is that it was able to accept or deliver charge more rapidly than the others, and the current level experienced by that cell was much higher. This is of concern because PCMs are generally designed assuming that equal current will be experienced by each cell, and therefore the maximum rated current of the PCM is calculated as the maximum rated current of each cell multiplied by the number of cells. Here, we see that the cells may take on uneven current levels, stressing cells having lower resistance. However, we expect that the extra stress of the higher current will tend to age that cell more quickly, causing its resistance to increase, ultimately leveling out the current experienced by each cell. That is, it may be a self-regulating phenomena.

The test was repeated (with different random resistances) for pack current having a 1C rate instead of a 10C rate. Results are plotted in Fig. 9. The disparity between peak current among cells in any given PCM is still relatively high.

Modeling resistance as a constant is inaccurate at high and low SOC. For the next simulations, a resistor model was used where resistance was 5mΩ at 0% and 100% SOC, and varied linearly with SOC between 0% and 50% SOC, and again be-

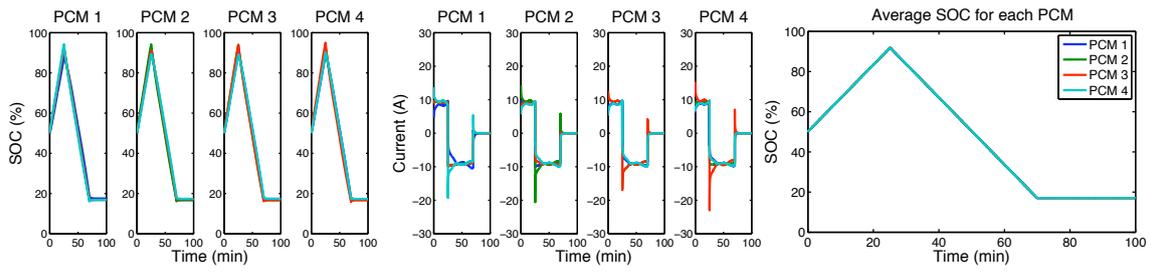


Figure 9: Cycling pack at 1C rate (random resistance values).

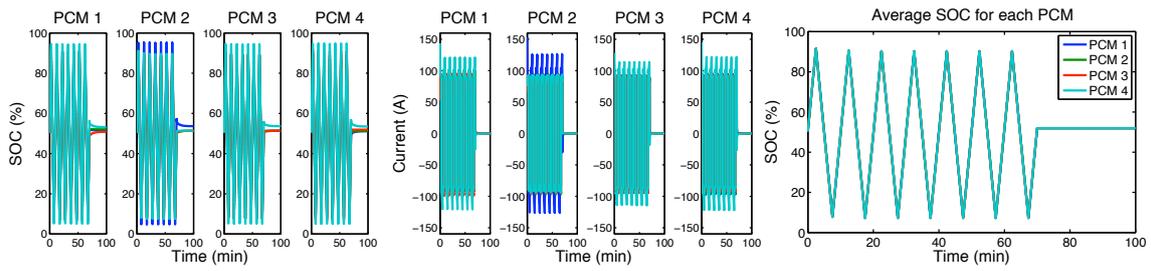


Figure 10: Cycling pack at 10C rate (random nonlinear resistance values).

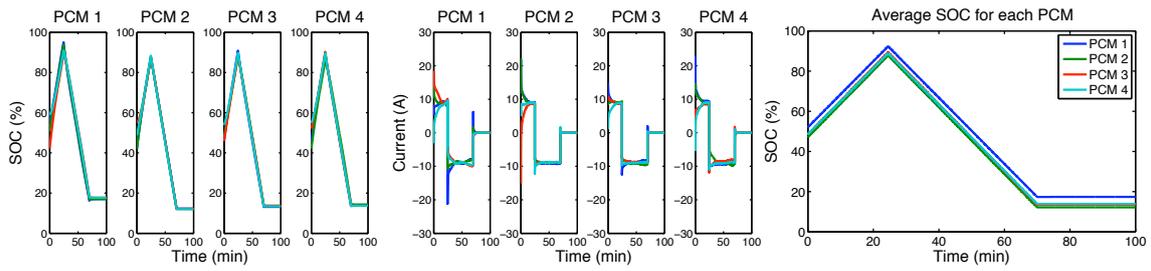


Figure 11: Cycling pack at 1C rate (random initial SOC, capacity and resistance values).

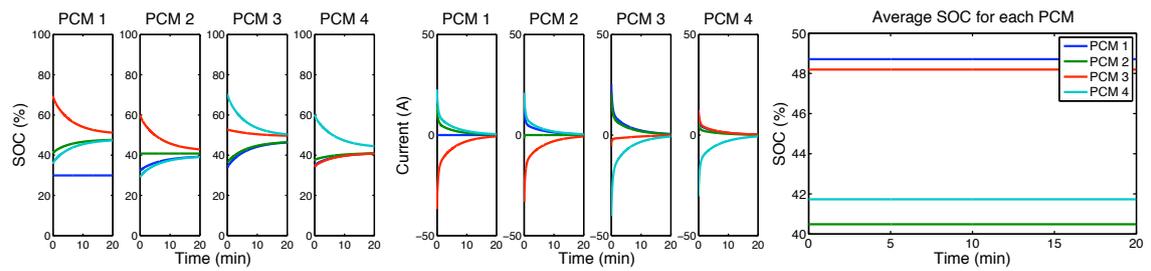


Figure 12: Resting pack (one cell in PCM 1 faulted open circuit).

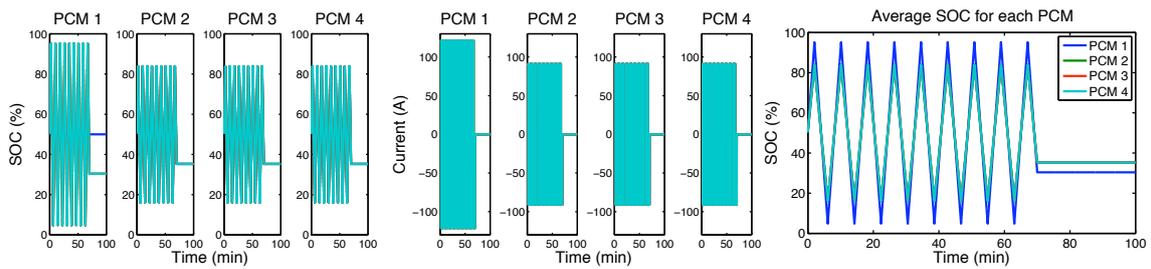


Figure 13: Cycling pack at 10C rate (one cell in PCM 1 faulted open circuit).

tween 50% and 100% SOC; the 50% SOC resistance value was randomly chosen between  $1\text{m}\Omega$  and  $4\text{m}\Omega$ . The current level was returned to 10C. Results are plotted in Fig. 10.

The main effect is that cells within a PCM do not diverge as far from each other. When one cell achieves either a much higher or much lower SOC value than others within that PCM, the resistance increases versus the others, so the cell does not change its SOC as quickly. In all cases, the PCM-average SOCs are essentially the same.

#### 4.5 Everything varies!

To see the total effect, when the initial SOC varies as above, and the initial capacity varies as above, and the cell resistance (constant versus SOC) varies as above, we ran one more simulation (with rate 1C). Results are plotted in Fig. 11. The effects are largely additive.

#### 4.6 Open-circuit fault

For the final PCM tests described in this paper, we consider some fault conditions. The first fault condition tested is for one cell in PCM 1 faulted open circuit. This eliminates that cell from the pack, so that all pack current must flow through the remaining three cells in that PCM. (Note that we have not observed cells failing in this way, but wanted to determine the effect on the pack should such a failure mode occur, perhaps if mechanical vibration broke a poor internal cell weld.) Results for this test, with different initial SOC values and no externally applied current are presented in Fig. 12.

Notice that one cell in PCM 1 has SOC that does not change. This is the cell that is faulted open circuit. That SOC value is not considered when computing the PCM SOC, since the associated voltage is not measurable. The rest of the pack behaves very like the first resting case considered in Fig. 4.

We next consider a pack with the same fault condition, but cycled at a 10C rate. Results are plotted in Fig. 13. As expected, the non-faulted cells in PCM 1 receive a much higher current level than the (non-faulted) cells in the other PCMs. This in turn causes their SOC values to change more rapidly than other cells, so that the average SOC for PCM 1 varies significantly more than that of other PCMs. The stress on the non-faulted cells in a PCM having an open-circuit fault will be much greater, possibly leading to a cascading failure of cells within a PCM. If all cells fail open-circuit, it is not possible to sustain pack current, and the pack fails. Note again, however, that we have not observed open-circuit faults to occur in operation. We do not presently know the likelihood or even the possibility of such a cascading failure.

#### 4.7 Short-circuit fault

One known failure mode for a cell is to develop an internal short circuit that results in the cell's SOC decreasing when there is no externally applied current. This phenomenon may be simply and reasonably modeled as a constant discharge current applied to the cell. What is unknown at this time, however, is what will happen when the

cell discharges below 0% SOC. Presumably, the cell will continue to self-discharge down to 0V. If the cell is subsequently charged, it is uncertain whether it will retain the charge, or will fault. The (overly simplistic but conservative) assumption of the simulator is that when a cell has SOC below 0%, it converts to a short-circuit fault.

Cells connected in parallel must maintain the same terminal voltage. Therefore, if one cell develops a leakage current, all other cells in that module will also have their SOC depleted. If one cell fails short-circuit, the other cells in the same PCM will also fail short-circuit. Note that this means that the pack will develop a lower overall terminal voltage due to the zero voltage of that PCM, but will still function.

Neglecting secondary effects, if the total leakage current in a module of cells is  $i_L$  amperes and the total capacity of the module is  $C$  ampere-hours, the time required for the module to self-discharge from 100% to 0% is  $C/i_L$  hours. Assuming that the pack can always be equalized so that all modules achieve 100% on full charge, a certain amount of leakage current is then manageable. That is, as long as the pack is recharged within a time interval less than  $C/i_L$ , the pack health will not degrade further. For example, if four 9 ampere-hour cells are connected in parallel to form a module, and the total leakage current is 0.1 amperes, then the pack must be recharged more frequently than once every  $36/0.1 = 360$  hours, or about every 15 days. (Of course, driving the vehicle will decrease the charge level of the pack, requiring an earlier recharge.)

Fig. 14 shows results from a simulation where one cell in PCM 1 has leakage current of 10 amperes. This is clearly an exaggeration, but helps show results in a moderate amount of time. All cells in the pack began the simulation with an SOC of 20%. There was no externally applied current. In the left and center plots of Fig. 14, the dark blue line corresponds to the cell having the leakage current in PCM 1; the coincident light blue lines correspond to the other cells.

We see that the SOC continuously decreases for the leaking cell, but not as quickly as if it were not connected in parallel with healthy cells. Once its SOC is different enough from the others in the same module to overcome voltage hysteresis, we see that the leakage current of cell 1 is offset by discharging currents in the connected cells (which attempt to recharge the leaking cell). A steady-state discharge current of about 10/4 amperes is achieved in all cells of PCM 1 (with second-order ripple effects caused by slightly different locations on the OCV curve, modulated by hysteresis and time constants). The cells discharge until the unhealthy cell reaches 0%. At this point, its OCV instantly changes to 0V (and its resistance is assumed to remain constant). A spike of current occurs as the healthy cells quickly discharge into this "short circuit", and then they too reach 0% SOC. By the end of the simulation, all cells in module 1 have short-circuited.

The transition behavior when a cell reaches 0% SOC is not completely accurate. Its OCV would not drop to 0% instantly. Therefore, we would

not expect this spike of current and immediate short-circuiting of the cell. However, if the cell is left to self-discharge for a very little time after it reaches 0%, we can expect it to fail, and that the cells connected in parallel to it would also fail. The next test considers the same scenario, but when there is an applied current to the pack. The pack is cycled at a 10C rate, and results are presented in Fig. 15.

We see that because of the leakage current in PCM 1, it never reaches the high SOC value reached by the other PCMs, and always reaches the low SOC value first. The pack cycling capacity effectively decreases over time. While the leakage current in this example is larger than reasonable, the same effect would be seen with any leakage current, over a longer time interval.

The next test considered cycling the pack at the same 10C rate, but with buck-only equalization “turned on”. PCMs with cells having SOC higher than the lowest cell SOC by at least 0.5% were bucked with a 10A constant-current load. Results are shown in Fig. 16.

In this example, we see that the bucking current causes the healthy cells to deplete their SOC at the same rate as the leaking cell, so the pack behaves uniformly (the average current in the center plot is negative). During cycling, the discharge period is shorter than the charge period due to the constant leakage current, but the pack can still operate. From this and similar simulations we conclude that leakage current can be managed as long as the rate of equalization is at least as large as the largest leakage current in the pack.

The remaining simulations consider what happens when the pack has encountered a true short-circuit fault. Fig. 17 shows the case of a pack initialized with different SOC values, where one cell in PCM 1 has a short-circuit fault. Voltages in PCMs 2–4 equalize as normal, and their SOCs also equalize. Voltages in PCM 1 are drawn down by the short-circuit fault. The effect is not instantaneous due to the resistances of the healthy cells. However, within a very short period of time, all cells in PCM 1 have faulted short circuit.

Fig. 18 shows a comparable result when the pack is cycled. The SOC of PCM 1 quickly drops to zero, and the SOC of the remaining PCMs cycles as normal. However, due to reduced pack voltage, to obtain a desired power level, the pack must be cycled at a higher current. Therefore, although losing cells short circuit does not cause the pack to stop functioning, it does place larger stresses on the remaining cells.

## 5 Simulation Results for SCM

This section discusses preliminary findings obtained by using the SCM simulator. Our biggest concern technically was whether we would see large SOC dispersion among different SCMs without some kind of active equalization (boost or buck circuitry) between the SCMs. For the SCM approach to be feasible, the SCMs must self-equalize to nearly the same SOC. (n.b., SOC is well defined for a single cell, but not well defined for a series-connected string of cells. Here,

we will use the average of all cell SOCs to indicate the SCM SOC, although this definition has some problems).

The following subsections present tests under various permutations of cell resistances, capacities, initial SOCs, and fault conditions, and under different cycling conditions. Unless otherwise stated, the pack being simulated comprised four SCMs, each having four cells.

### 5.1 The pack at rest

If cells are initialized to disparate SOCs, and no external current is sourced/sunk by the pack, we would expect a degree of self-equalization between the SCMs, as the combined lumped voltages of the different SCMs would not be the same. Each SCM would then behave something like an RC (resistor-capacitor) circuit, whereby the SOCs of the SCMs adjust so that the combined lumped voltage of each SCM is equal. Small resistances allow larger currents (for the same voltage difference) and hence faster adjustment; larger resistances cause slower adjustment. The first test run using the simulator was of a resting pack, to confirm this expectation and to test the sanity of the simulator results. It is also indicative of how SCMs will self-equalize within a pack should their total voltages differ when they are initially connected

Fig. 19 illustrates typical results where SOC for each cell is randomly initialized within 25% and 75%, where all cell capacities are the same and all cell resistances are the same.

First, we comment that in this test intra-SCM equalization is “off” (no individual cell “boost” or “buck” circuitry). Therefore, since all cells have the same capacity, and the current passing through all cells in an SCM is the same, all cell SOCs within any SCM move together. That is, within any given SCM, cells maintain their relative separation in SOC. This effect is evident in the left figure. Secondly, due to random initial cell SOCs, the initial SCM OCVs differ. SCMs with higher OCV will source a current that is sunk by SCMs with lesser OCV. Therefore, we expect a kind of balancing of the various SCM-average SOCs. The right figure confirms that this is happening. However, due to the nonlinear relationship of the SOC versus OCV curve, when the SCM OCVs converge to the same value, the SCM-average SOCs do not converge to the same value—only to within a neighborhood of the same value.

Fig. 20 addresses the same scenario, but when intra-SCM equalization is “turned on.” Any cells in an SCM whose SOC is higher than the lowest SOC in that SCM by at least 0.5% has its charge level reduced. This is accomplished by individually draining current out of that cell at a constant 1A rate (and would be accomplished using a switched resistor in practice). The 1A rate is higher than we would expect to see in a practical application, but allows us to rapidly see the effects of equalization in the simulation. Here we see that all cells in all SCMs converge to the same approximate level by independently equalizing the local cells (that is, no SCM required knowledge from any other SCM).

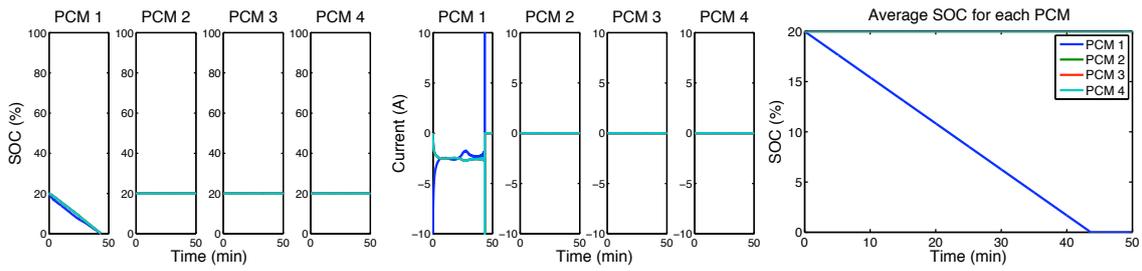


Figure 14: Resting pack (one cell in PCM 1 leaking at 10A rate.).

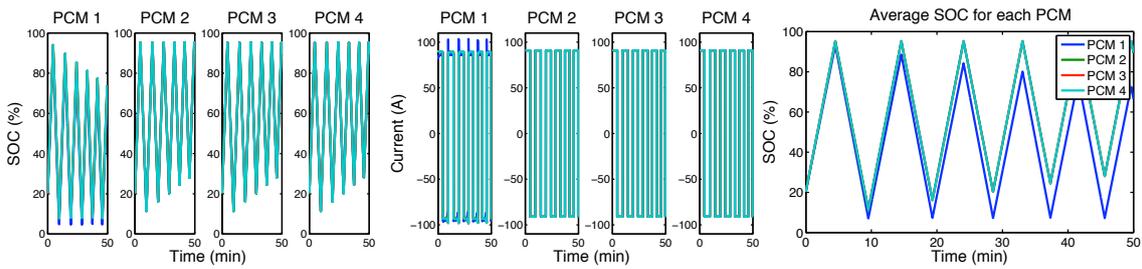


Figure 15: Cycling pack at 10C rate (one cell in PCM 1 leaking at 10A rate).

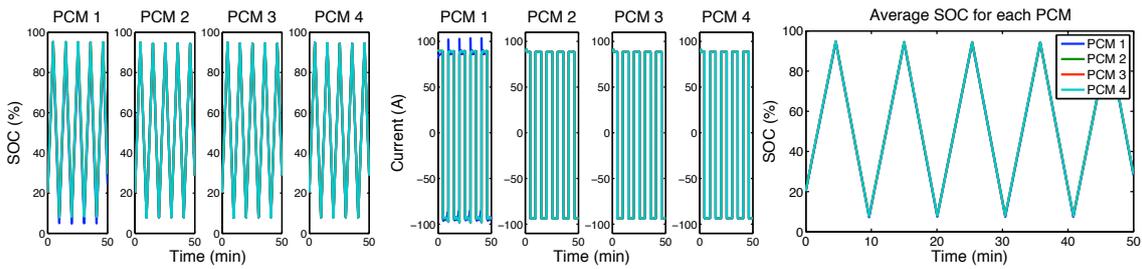


Figure 16: Cycling pack at 10C rate (one cell in PCM 1 leaking at 10A rate; equalization of 10A “on”).

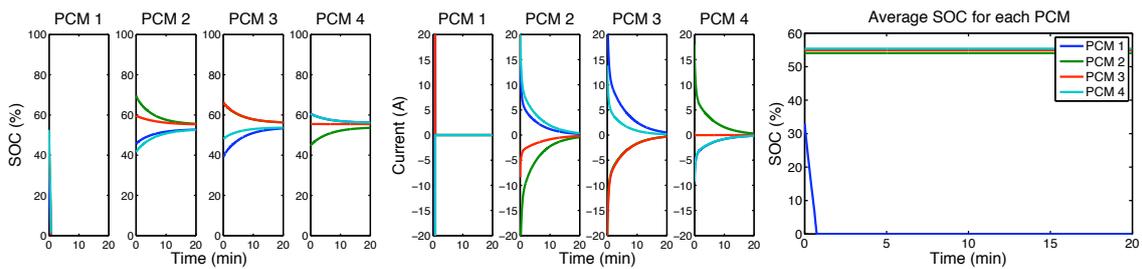


Figure 17: Resting pack (one cell in PCM 1 faulted short circuit).

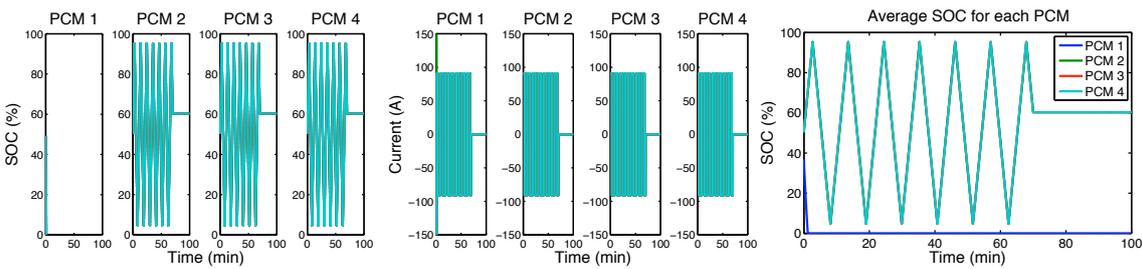


Figure 18: Cycling pack at 10C rate (one cell in PCM 1 faulted short circuit).

These results are not dependent on cell resistance (except in terms of time scale). Varying cell capacity has an effect, but the same general result holds that a resting pack will have SCM SOC that converge to the same neighborhood.

## 5.2 Varying initial SOC

The second SCM test that we consider maintains a constant resistance and a constant capacity per cell, again initializes each cell with a random SOC, but then cycles the pack with constant-current charge and discharge pulses. The magnitude of the pulses used in the simulation is 10C (about 360A). While a 10C pulse is quite large, especially if an EV pack is being considered, it speeds the simulation. In certain cases the higher current can lead to magnified effects, as we will see later, but that is not the case here. (Charging was stopped when the maximum cell SOC reached 95%, and discharging stopped when the minimum cell SOC reached 5%). After 10 min, the pack was allowed to rest. Results typical of this scenario are presented in Fig. 21.

The most important aspects of these results are essentially identical to those of the “rest” case just presented. Namely, the SCM SOC converge to values close to each other, even in a dynamic setting. (When equalization is turned on, the results were essentially the same, except that the intra-SCM SOC deviation slowly decreases, leading to inter-SCM SOC deviation decreasing as well.)

## 5.3 Varying capacity

The third test that we consider maintains a constant resistance and initial SOC (of 50%) for each cell, but gives each cell a random capacity uniformly chosen between 8.5Ah and 9.5Ah. The pack is then cycled, and results are plotted in Fig. 22.

While all cell SOC start with the same value, due to differing cell capacities they diverge in value as the SCM SOC approach their upper and lower limits. In this case, the magnitude of the divergence is around 0.8%.

Decreasing the pulse constant-current level from 10C to 1C had an interesting effect. Within SCMs, there is still a variance in the SOC of the various cells, but that the parallel-connected SCMs tend to balance out the composite SCM-average SOC. It was easier to accomplish this with the lower pack current (which tends to de-equalize the SCMs) because relatively more “equalizing” could be done—the rate of inter-SCM equalization is unchanged, but the rate of de-equalization was reduced. We see that the overall level of SCM SOC disparity is much less than before.

## 5.4 Varying resistance

The fourth SCM test that we consider maintains a constant capacity and initial SOC (of 50%) for each cell, but varies the resistance. The simulator permits very complex models of resistance as a function of SOC, but we begin here with the assumption that resistance is constant but different for each cell, distributed uniformly between 1m $\Omega$  and 4m $\Omega$ . We again begin with a high-rate

simulation, as shown in Fig. 23.

While cycling, all cells within an SCM maintain identical SOC because of identical capacity and initial SOC. The SCM-average SOC differ because of the different SCM resistances, such that each SCM accepts a different fraction of the pack dis/charge current. However, when the pack is allowed to rest, the difference between SCM-average SOC converges to zero. With reduced current (1C versus 10C), we get the results of Fig. 24.

Here, the de-equalizing pack current is relatively smaller, so the equalizing inter-SCM current is better able to keep the SCMs balanced. Total SOC divergence is less. Again, the pack recovers when allowed to rest.

Modeling resistance as a constant is inaccurate at high and low SOC. For the next simulations, a resistor model was used where resistance was 5m $\Omega$  at 0% and 100% SOC, and tapered down to a random value between 1m $\Omega$  and 4m $\Omega$  at 50% SOC. The current level was returned to 10C, and results are shown in Fig. 25.

The SOC divergence was better. Higher resistances at extreme SOC tended to limit the current in a particular SCM versus the others, allowing less extreme SCM-average SOC swings as the pack was charged and discharged. Constant resistance versus SOC should be treated as worst-case.

## 5.5 Everything varies!

To see the total effect, when the initial SOC varies as above, and the initial capacity varies as above, and the cell resistance (constant versus SOC) varies as above, we ran one more simulation (with rate 10C). Results are shown in Fig. 26.

The effects are largely additive, with maximum SOC divergence being worse than before, and the difference in SCM-average resting SOC not converging to zero because of the different initial SOC. The above simulation was done for a 10C rate, the following for a 1C rate. Results are plotted in Fig. 27. Again, the effect is much lower.

## 5.6 Open-circuit fault

For the final SCM tests described in this paper, we consider some fault conditions. The first fault condition tested is for one cell in SCM 1 faulted open circuit. This eliminates that SCM from the pack. (Note that we have not observed cells failing in this way, but wanted to determine the effect on the pack should such a failure mode occur.) Results for the resting test are presented in Fig. 28.

We see very similar behavior to the other resting tests, but with one fewer SCM to consider (the average SOC of the faulted SCM is not considered in the third figure since it does not contribute to the pack’s performance). For the 10C-rate case with random everything but with a cell in SCM 1 faulted open-circuit, the results are plotted in Fig. 29.

We see similar results to the non-faulted case. Note, however, (1) The overall pack current is now split into three SCMs rather than four, resulting in a higher relative C-rate for each SCM.

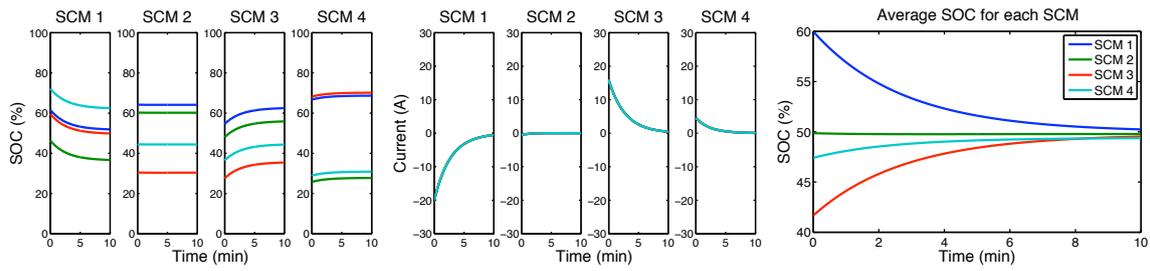


Figure 19: Resting pack (random initial SOC values).

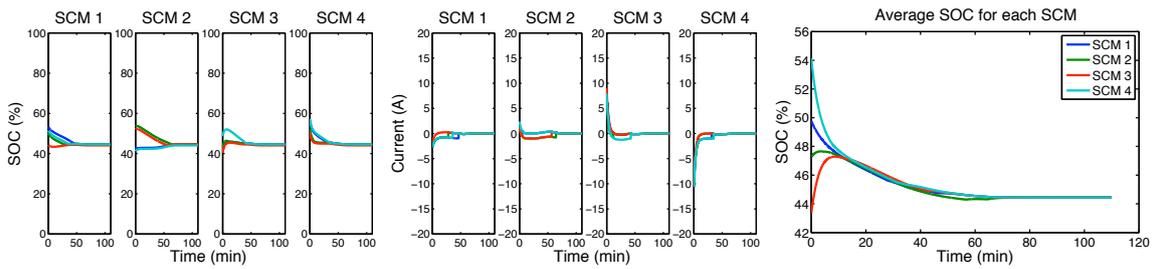


Figure 20: Resting pack with intra-SCM equalization "on" (random initial SOC values).

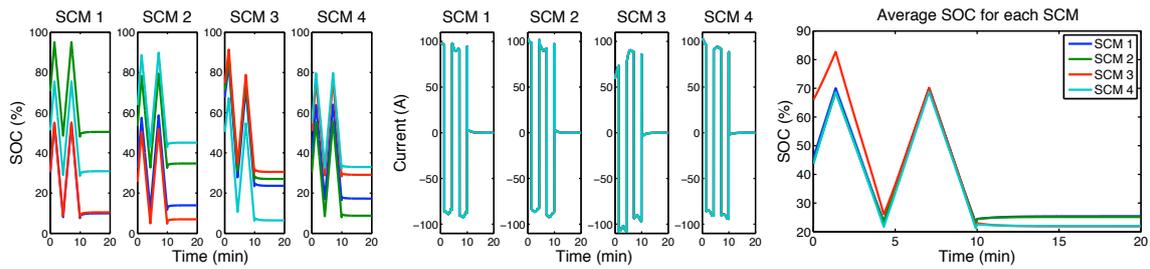


Figure 21: Cycling pack at 10C rate (random initial SOC values).

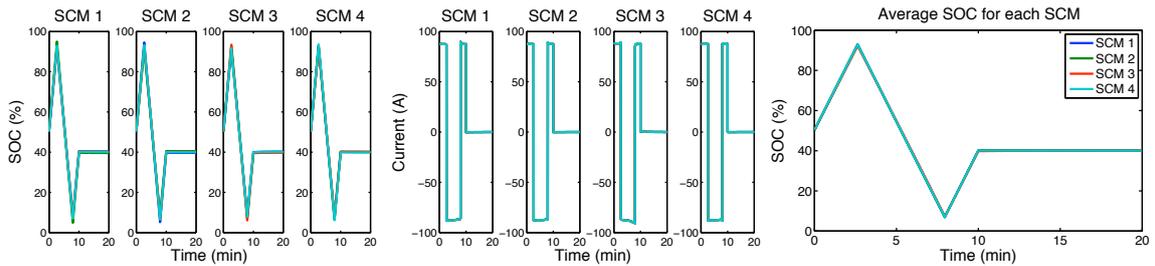


Figure 22: Cycling pack at 10C rate (random initial capacity values).

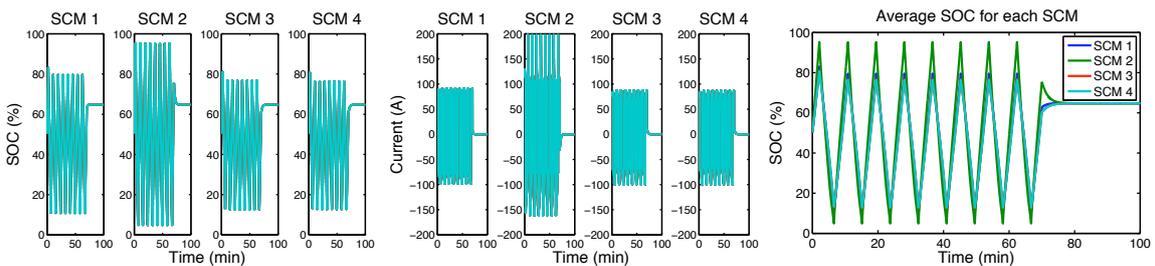


Figure 23: Cycling pack at 10C rate (random resistance values).

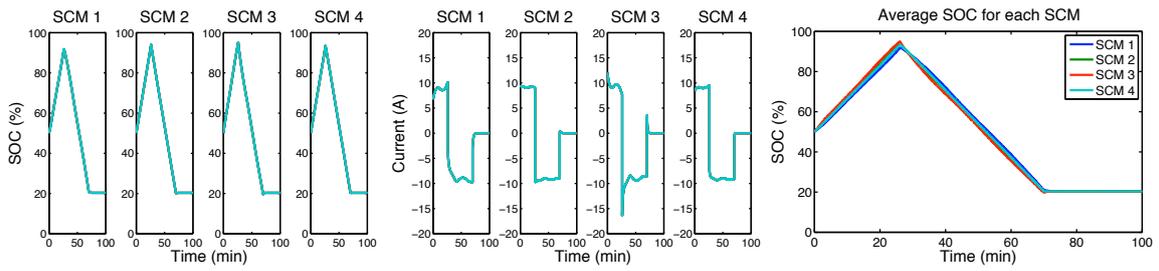


Figure 24: Cycling pack at 1C rate (random resistance values).

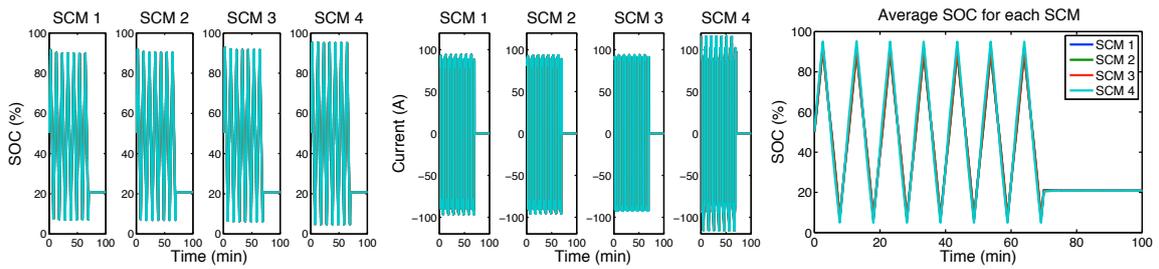


Figure 25: Cycling pack at 10C rate (random nonlinear resistance values).

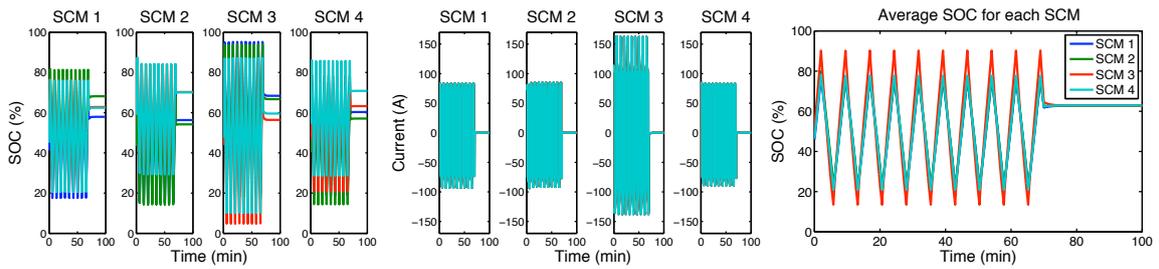


Figure 26: Cycling pack at 10C rate (random initial SOC, capacity and resistance values).

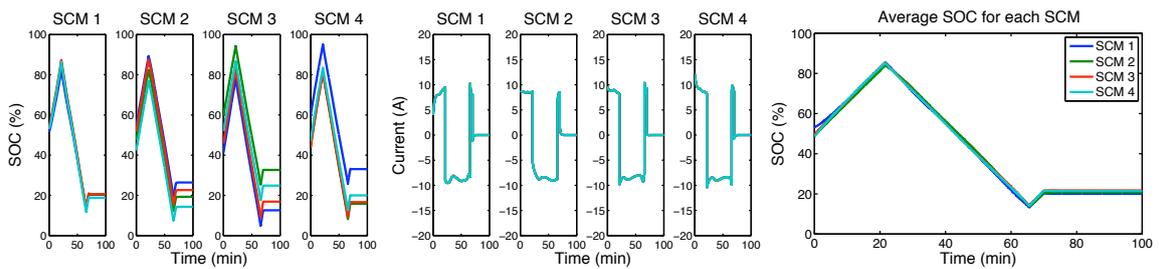


Figure 27: Cycling pack at 1C rate (random initial SOC, resistance and capacity values).

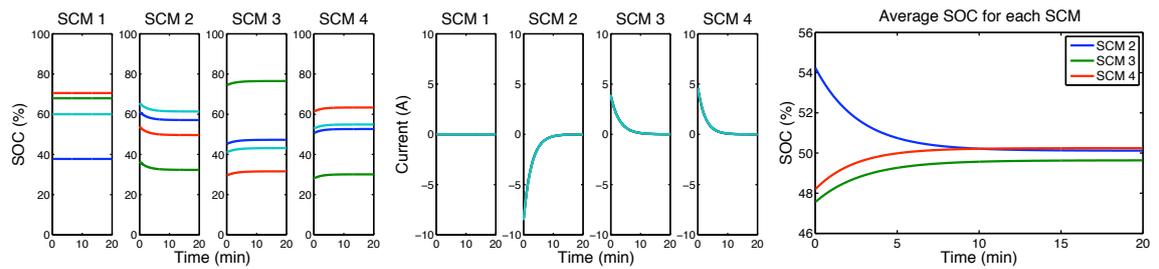


Figure 28: Resting pack (one cell in SCM 1 faulted open circuit).

This increases the dynamic imbalance of the pack, and (2) cycling is faster due to the higher relative C-rates, meaning that the overall EV range (for example) is reduced due to the faulted SCM being removed from the pack.

### 5.7 Short-circuit fault

The second faulted condition that we consider is the effect of a single cell in SCM 2 that has faulted short-circuit. (This is a cell failure mode that we have observed, particularly after over-discharging the cell.) That SCM then has one fewer cell than the other SCM in terms of developing the required bus voltage. We expect that the SOCs in that SCM must then be higher to compensate, limiting pack cycling capability since they will reach an upper SOC limit before other cells in other SCMs will, but never achieving the SOC lower limit. In order to conduct these tests in a meaningful way, we had to increase the number of cells in each SCM so that the voltage lost by the short-circuit cell (nominally 3.75V) could be compensated for by the other cells in the SCM. In the following tests, 96 cells per SCM were used. The first test was a rest test—resistances, capacities, and initial SOCs were initialized randomly, and the pack was allowed to rest. Results are plotted in Fig. 30.

As expected, we see that the individual cell SOCs in SCMs 1, 3, and 4 are decreasing to give a lower bus voltage, and the SOCs in SCM 2 are increasing to match that voltage with only 95 cells. The right figure makes this very clear. In this case, the steady-state SOC difference was about 7.5% versus 0.5% in the first rest case with unfaulted cells—the results are not directly comparable, but we do see a significant difference in resting SOC difference that is repeatable in character—the exact value of difference can be explored in a more scientific study. In Fig. 31, we present similar results to the above, except that the pack was cycled at 10C.

We again see a significant difference in SOC in the rest state, due mostly to the single faulted cell. This single faulted cell has removed roughly 8% of the pack's cycling ability, measured by SOC range. To get an idea what two short-circuit cells might do, we ran one last resting test, plotted in Fig. 32. The effect is roughly doubled.

## 6 Summary

When designing battery pack configurations, it is important to understand the consequences of different design decisions. This paper gives some economic tradeoffs between PCM and SCM and then describes simulators created to better understand packs comprising parallel-cell-modules or series-cell modules.

### Some of the main findings for PCM are:

- Most pack abnormalities are self-correcting to a large extent. That is, differences among capacities and resistances (for example) are averaged out (in steady state) over the cells comprising a particular PCM.
- Transient behavior is still affected by these differences. However, even for extreme variation

in resistance and capacity, the pack remained very usable. Any period where the pack experiences a low current demand will allow the transient effects to die out.

- The biggest concern is that of leakage current. We don't presently understand what happens when a cell's SOC drops below 0%, but assume that it can cause permanent damage and eventually lead to a cell fault (further assumed to be short-circuit fault).
- Cell faults due to leakage current can be avoided if the pack is recharged sufficiently often, and the pack maintains useful capacity if equalization of PCM SOC values can happen more quickly than the worst-case PCM "leaks" current. For resting packs, the inter-recharge period is on the order of  $C/i_L$ , where  $C$  is the module capacity and  $i_L$  is the leakage current, but this time decreases if the pack is discharged (due to use). Paralleling cells actually helps extend this period since the module capacity is the sum of cell capacities.
- If cells with SOC below 0% do in fact develop short-circuit faults, then any cell developing that fault will cause all other cells in that module to develop the same fault. However, the pack is still operational, but with lower terminal voltage (and therefore lower power).

### Some of the main findings for SCM are:

- The pack exhibits a self-balancing effect during intervals when the pack is resting (no externally applied current). The average SOC of each series SCM will converge to a constant value as the total of all OCVs in the SCM converges to a constant bus voltage. However, because the OCV versus SOC relationship is nonlinear, when the bus voltage converges, the SCM-average SOCs will not all converge to exactly the same level.
- When the pack is exercised (externally applied current is nonzero), the level of SOC dispersion between SCM-average SOCs varies. Two effects are present: (1) the self-balancing effect of the pack, and (2) the disturbing effect of the applied current. As the level of externally applied current increases, so too the dispersion between SCM-average SOCs because the pack cannot balance itself quickly enough to compensate. For reasonable levels of externally applied current, the overall effect of dispersion was not large. When the pack subsequently rests, the SOCs converge as in the first case.
- When an SCM has a cell that has faulted open-circuit, that entire SCM is removed from the pack electrically. The remaining SCMs operate together just like a non-faulted pack, although they take a higher individual load to deliver the same power.
- When an SCM has a cell that has faulted short-circuit, that SCM must match the pack bus voltage with effectively one fewer cell doing so. Therefore, that SCM's average SOC must be higher than those of the other SCMs. In an

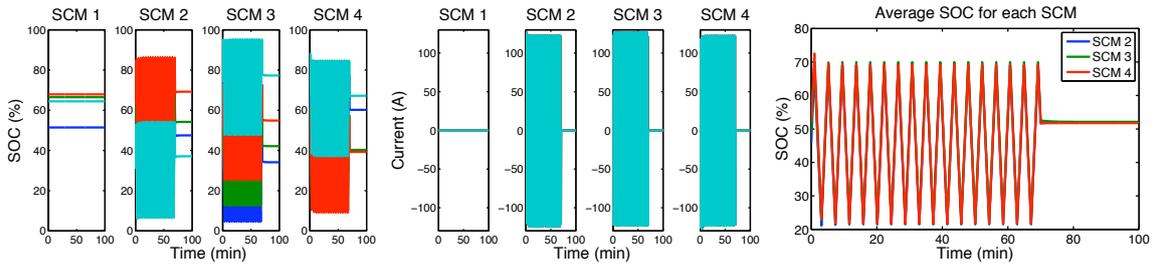


Figure 29: Cycling pack at 10C rate (one cell in SCM 1 faulted open circuit).

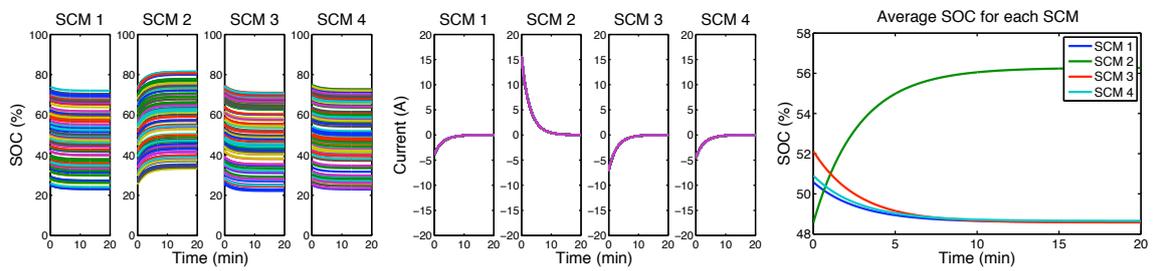


Figure 30: Resting pack (one cell in SCM 2 faulted short circuit).

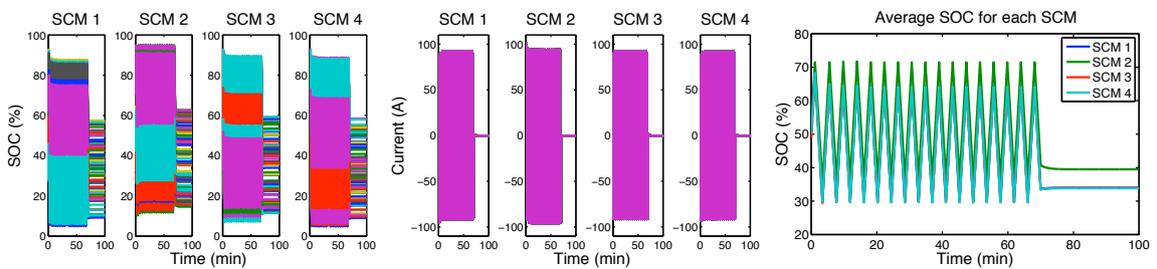


Figure 31: Cycling pack at 10C rate (one cell in SCM 2 faulted short circuit).

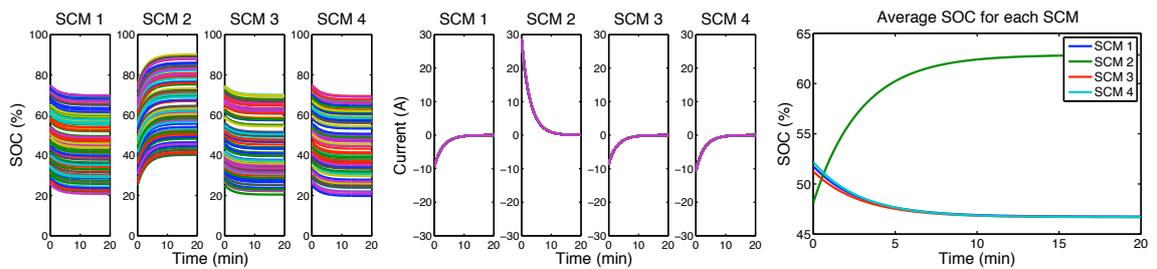


Figure 32: Resting pack (two cells in SCM 2 faulted short circuit).

application where the SOC swing is used to determine performance (e.g., an EV, where SOC swing determines range), this will start limiting performance very quickly.

- In most of the simulations herein, cells within individual SCMs were not balanced in order to better illustrate worst-case effects. True packs would be better balanced. However, the above-mentioned “balancing effect” does not balance cells within SCMs, only the SCM-average SOC of each SCM, so that individual cell equalization will still be required.
- The largest “caution” flags to date are for situations where cells are faulted in a short-circuit modality. The remaining cells in that SCM must achieve the bus voltage, raising their SOC vis-à-vis the cells in other SCMs. This limits the overall dynamic range of pack performance. It may be wise to include a contactor for each SCM, to “switch out” one or more degraded SCMs until such time that all SCMs are degraded, and to then “switch them back in”. This requires future investigation.

In summary, both the PCM and SCM approaches have advantages and disadvantages, but both appear viable. Most implementations will likely comprise modules having some combination of cells wired in series and in parallel. Due to the higher component costs of SCM, we expect that most light-duty high-volume applications will tend toward a PCM dominated approach, but an SCM dominated approach may make sense for heavy-duty low-volume applications where it would be difficult to recover non-recurring engineering costs associated with designing separate high voltage packs having multiple capacity options.

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